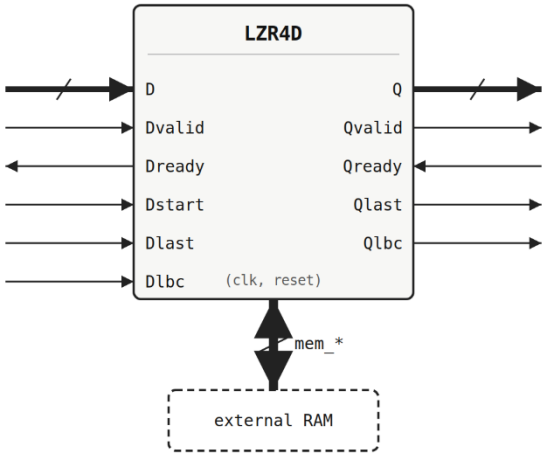
LZR4D Core

Ultralow-Latency Single-Engine Decompressor Core

The LZR4D core implements lossless decompression of data compressed in the LZ4 format. Unlike conventional few-bytes-per-clock or token-per-clock designs, the LZR4D resolves multiple LZ4 sequences concurrently within a single decompression engine, sustaining an output rate of 256 bits (32 bytes) of decompressed data per clock cycle on a single compressed stream. At the multi-gigahertz clock rates of advanced process nodes, this corresponds to terabit-class decompression throughput in a single engine, with no need to split data into independently compressed blocks across an array of slower decompressors.

The core's decompression latency is below 30 clock cycles, which translates to an end-to-end decompression delay of 10 to 20 nanoseconds in advanced semiconductor nodes. This ultralow, deterministic latency allows the LZR4D to be placed directly in latency-critical data paths, such as compressed memory tiers, CXL-attached memory expanders, solid-state storage controllers, enterprise storage appliances, and in-network data processing, where the decompression step was previously a bottleneck.

Symbol



Key Features

- Single-engine architecture sustains 256 bits (32 bytes) of decompressed output per clock cycle
- Terabit-class decompression throughput at multi-gigahertz clock frequencies
- Ultralow, deterministic latency of under 30 clock cycles (10 to 20 ns in advanced semiconductor nodes)
- Resolves multiple LZ4 sequences concurrently within a single decompression engine
- No block-level stream splitting or arrays of parallel engines required
- Suitable for placement directly in latency-critical data paths

Applications

- Compressed memory tiers
- CXL-attached memory expanders
- Solid-state storage controllers
- Enterprise storage appliances
- In-network data processing
- Network processors and memory subsystems

Pin Description

Name	Type	Description
CLK	Input	Core clock signal
RESET	Input	HIGH level asynchronously resets the core
D	Input	Compressed input data bus, 8 bits width
Dvalid	Input	Data on D is valid
Dready	Output	Core is ready to accept data on D
Dstart	Input	Indicates the start of a new compressed frame on D
Dlast	Input	Indicates the last beat of the compressed frame on D
Dlbc	Input	Valid byte count in the last beat of D
Q	Output	Decompressed output data bus, 256 bits wide
Qvalid	Output	Data on Q is valid
Qready	Input	Indicates downstream is ready to accept data on Q
Qlast	Output	Indicates the last beat of the decompressed frame on Q
Qlbc	Output	Valid byte count in the last beat of Q
mem_*	Bidirectional	External RAM interface used by the decompression engine

Deliverables

HDL Source Licenses

- Synthesizable Verilog RTL source code
- Verilog testbench (self-checking)
- Vectors for the testbench
- Expected results
- User Documentation

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